What is Claimed is:

1. A programmable logic device comprising:

input-output circuitry having differential input drivers and differential output drivers; and

programmable core logic that produces data signals for the input-output circuitry and that receives data signals from the input-output circuitry, wherein the input-output circuitry comprises:

input driver common-mode-voltage bias circuitry that adjusts common-mode-voltage levels at the input drivers; and

output driver common-mode-voltage bias circuitry that adjusts common-mode-voltage levels at the output drivers.

2. The programmable logic device defined in claim 1 wherein at least a given one of the input drivers has a differential input driver circuit with two differential inputs, wherein the two differential inputs are bridged by two resistors that are separated by an input driver node, and wherein the input driver common-mode-voltage bias circuitry is connected to the input driver node.

3. The programmable logic device defined in claim 1 wherein:

at least a given one of the input drivers has a differential input driver circuit with two

differential inputs;

the two differential inputs are bridged by two resistors that are separated by an input driver node;

the input driver common-mode-voltage bias circuitry is coupled to the input driver node;

the input driver common-mode-voltage bias circuitry comprises an adjustable resistor; and

the adjustable resistor is connected to the input driver node.

4. The programmable logic device defined in claim 1 wherein:

at least a given one of the input drivers has a differential input driver circuit with two differential inputs;

the two differential inputs are bridged by two resistors that are separated by an input driver node;

the input driver common-mode-voltage bias circuitry is coupled to the input driver node;

the input driver common-mode-voltage bias circuitry comprises an adjustable resistor; and

the adjustable resistor is connected to the input driver node, the programmable logic device further comprising dynamic control circuitry that generates dynamic control signals, wherein at least some of the dynamic control signals control the adjustable resistor.

5. The programmable logic device defined in claim 1 wherein:

at least a given one of the input drivers has a differential input driver circuit with two differential inputs;

the two differential inputs are bridged by two resistors that are separated by an input driver node;

the input driver common-mode-voltage bias circuitry is coupled to the input driver node;

the input driver common-mode-voltage bias circuitry comprises an adjustable resistor; and

the adjustable resistor is connected to the input driver node, the programmable logic device further comprising static control circuitry having programmable elements that generate static control signals, wherein at least some of the static control signals control the adjustable resistor.

6. The programmable logic device defined in claim 1 wherein:

at least a given one of the input drivers has a differential input driver circuit with two differential inputs;

the two differential inputs are bridged by two resistors that are separated by an input driver node;

the input driver common-mode-voltage bias

circuitry is coupled to the input driver node;

the input driver common-mode-voltage bias circuitry comprises an adjustable resistor; and

the adjustable resistor is connected to the input driver node, the programmable logic device further comprising programmable random-access-memory cells that generate static control signals, wherein at least some of the static control signals control the adjustable resistor.

7. The programmable logic device defined in claim 1 wherein:

at least a given one of the input drivers has a differential input driver circuit with two differential inputs;

the two differential inputs are bridged by two resistors that are separated by an input driver node;

the input driver common-mode-voltage bias circuitry is coupled to the input driver node;

the input driver common-mode-voltage bias circuitry comprises an adjustable resistor and an adjustable current source; and

the adjustable resistor and adjustable current source are connected to the input driver node.

8. The programmable logic device defined in claim 1 wherein at least a given one of the output drivers has a differential output driver circuit with

two differential outputs, wherein the two differential outputs are bridged by two resistors that are separated by an output driver node, and wherein the output driver common-mode-voltage bias circuitry is connected to the output driver node.

9. The programmable logic device defined in claim 1 wherein:

at least a given one of the input drivers has a differential input driver circuit with two differential inputs;

the two differential inputs are bridged by two input driver resistors that are separated by an input driver node;

the input driver common-mode-voltage bias circuitry is connected to the input driver node;

at least a given one of the output drivers has a differential output driver circuit with two differential outputs;

the two differential outputs are bridged by two output driver resistors that are separated by an output driver node; and

the output driver common-mode-voltage bias circuitry is connected to the output driver node.

10. The programmable logic device defined in claim 1 wherein:

at least a given one of the output drivers has a differential output driver circuit with

two differential outputs;

the two differential outputs are bridged by two resistors that are separated by an output driver node;

the output driver common-mode-voltage bias circuitry is coupled to the output driver node;

the output driver common-mode-voltage bias circuitry comprises an adjustable resistor; and

the adjustable resistor is connected to the output driver node.

11. The programmable logic device defined in claim 1 wherein:

at least a given one of the output drivers has a differential output driver circuit with two differential outputs;

the two differential outputs are bridged by two resistors that are separated by an output driver node;

the output driver common-mode-voltage bias circuitry is coupled to the output driver node;

the output driver common-mode-voltage bias circuitry comprises an adjustable resistor; and

the adjustable resistor is connected to the output driver node, the programmable logic device further comprising static and dynamic control circuitry that generates static and dynamic control signals, wherein at least some of the static and dynamic control signals control the adjustable resistor.

12. The programmable logic device defined in claim 1 wherein:

at least a given one of the output drivers has a differential output driver circuit with two differential outputs;

the two differential outputs are bridged by two resistors that are separated by an output driver node;

the output driver common-mode-voltage bias circuitry is coupled to the output driver node;

the output driver common-mode-voltage bias circuitry comprises an adjustable resistor and an adjustable current source; and

the adjustable resistor and adjustable current source are connected to the output driver node.

13. The programmable logic device defined in claim 1 wherein:

at least a given one of the input drivers has a differential input driver circuit with two differential inputs;

the two differential inputs are bridged by two input driver resistors that are separated by an input driver node;

the input driver common-mode-voltage bias circuitry is coupled to the input driver node;

the input driver common-mode-voltage bias circuitry comprises an adjustable input driver common-

mode-voltage bias circuit resistor and an adjustable input driver common-mode-voltage bias circuit current source;

the adjustable input driver common-mode-voltage bias circuit resistor and adjustable input driver common-mode-voltage bias circuit current source are connected to the input driver node;

at least a given one of the output drivers has a differential output driver circuit with two differential outputs;

the two differential outputs are bridged by two output driver resistors that are separated by an output driver node;

the output driver common-mode-voltage bias circuitry is coupled to the output driver node;

the output driver common-mode-voltage bias circuitry comprises an adjustable output driver common-mode-voltage bias circuit resistor and an adjustable output driver common-mode-voltage bias circuit current source;

the adjustable output driver common-mode-voltage bias circuit resistor and output driver common-mode-voltage bias circuit adjustable current source are connected to the output driver node; and

the output driver common-mode-voltage bias circuitry and input driver common-mode-voltage bias circuitry are separately adjustable.

14. An integrated circuit differential driver

on an integrated circuit that communicates with another integrated circuit using a differential communications path over which differential data signals are conveyed, comprising:

a differential driver that is connected to the differential communications path and through which the differential data signals are passed, wherein the differential driver has a desired common-mode-voltage operating range; and

adjustable common-mode-voltage bias circuitry coupled to the differential driver that is adjusted so that the differential data signals passing through the differential driver have a common-mode voltage level within the desired common-mode-voltage operating range, wherein the common-mode-voltage bias circuitry comprises an adjustable resistor and an adjustable current source that are controlled by static control signals provided on the integrated circuit.

15. The integrated circuit differential driver defined in claim 14 wherein the differential driver comprise an input driver having two differential inputs and having two resistors that bridge the two differential inputs, wherein the two resistors are separated by a node to which the adjustable common-mode-voltage bias circuitry is connected.

16. The integrated circuit differential driver defined in claim 14 wherein the differential

driver comprise an output driver having two differential outputs and having two resistors that bridge the two differential outputs, wherein the two resistors are separated by a node to which the adjustable common-mode-voltage bias circuitry is connected.

17. The integrated circuit differential driver defined in claim 14 wherein the adjustable resistor and adjustable current source each include transistors that are independently adjustable by the static control signals, so that the adjustable resistor is adjustable to produce a resistance value independent of what level of current is produced by the adjustable current source.

18. The integrated circuit differential driver defined in claim 14 wherein the adjustable resistor produces an adjustable resistance, wherein the adjustable current source produces an adjustable bias current, and wherein the adjustable current source and adjustable resistor are controlled by the same static control signals so that the adjustable resistance cannot be adjusted independently from the adjustable bias current.

19. The integrated circuit differential driver defined in claim 14 wherein the adjustable resistor produces an adjustable resistance, wherein the adjustable current source produces an adjustable bias

current, and wherein the adjustable current source and adjustable resistor comprise a plurality of current mirror branch sections each having an associated resistor and each having at least one transistor controlled by a respective one of the static control signals, wherein the static control signals turn the transistors on and off to simultaneously adjust the adjustable resistance and the adjustable bias current.

20. An integrated circuit common-mode-voltage bias circuit on an integrated circuit that produces an output signal at an output terminal that is used in adjusting a common-mode voltage level associated with differential data signals passing through a differential driver on the integrated circuit, the bias circuit comprising:

a reference section that produces a reference current;

a plurality of current mirror transistors arranged in a plurality of current mirror branch sections, each current mirror branch section having an associated current level that is a multiple of the reference current;

a plurality of resistors, each resistor being coupled to one of the current mirror transistors;

control transistors that switch the current mirror transistors and resistors into or out of the bias circuit to adjust the output signal produced at the output terminal; and

a plurality of programmable random-access memory cells that produce static control signals, wherein the control transistors are each coupled to one of the programmable random-access memory cells and are turned on or off by the static control signals.

21. An integrated circuit common-mode-voltage bias circuit on an integrated circuit that produces an output signal at an output terminal that is used in adjusting a common-mode voltage level associated with differential data signals passing through a differential driver on the integrated circuit, wherein the integrated circuit includes dynamic control circuitry, the bias circuit comprising:

a reference section that produces a reference current;

a plurality of current mirror transistors arranged in a plurality of current mirror branch sections, each current mirror branch section having an associated current level that is a multiple of the reference current;

a plurality of resistors, each resistor being coupled to one of the current mirror transistors; and

control transistors that switch the current mirror transistors and resistors into or out of the bias circuit to adjust the output signal produced at the output terminal, wherein the control transistors receive dynamic control signals from the dynamic control

circuitry on the integrated circuit and wherein the dynamic control signals turn the control transistors on and off.

22. A method of using first and second programmable logic device integrated circuits of a single given type in AC-coupled and DC-coupled differential communications environments, wherein each programmable logic device integrated circuit of the given type has a differential driver that is used to communicate over a differential communications link and has common-mode-voltage bias circuitry for making common-mode-voltage adjustments at the differential driver, the method comprising:

in an AC-coupled environment in which the differential communications link has DC-blocking capacitors:

using a first programmable logic device integrated circuit of the given type to communicate with another integrated circuit over the differential communications link; and

using the common-mode-voltage bias circuitry in the first programmable logic device to make common-mode-voltage adjustments at the differential driver in the first programmable logic device integrated circuit that optimize the performance of that differential driver without regard to what common-mode voltage is desired for the other integrated circuit;

in a DC-coupled environment in which the

differential communications link has no DC-blocking capacitors:

using a second programmable logic device integrated circuit of the same given type to communicate over the differential communication link with an additional integrated circuit; and

using the common-mode-voltage bias circuitry in the second programmable logic device to make common-mode-voltage adjustments at the differential driver in the second programmable logic device while taking into account which common-mode-voltage changes result at the additional integrated circuit due to the common-mode-voltage adjustments made by the common-mode-voltage bias circuitry of the second programmable logic device.

23. The method defined in claim 22 further comprising, while taking into account which common-mode-voltage changes result at the additional integrated circuit due to the common-mode-voltage adjustments made by the common-mode-voltage bias circuitry of the second programmable logic device, using the common-mode-voltage bias circuitry of the second programmable logic device to reduce contention current along the differential communications path to reduce DC power consumption.

24. The method defined in claim 22 further comprising, while taking into account which common-mode-voltage changes result at the additional integrated

circuit due to the common-mode-voltage adjustments made by the common-mode-voltage bias circuitry of the second programmable logic device, using the common-mode-voltage bias circuitry of the second programmable logic device to improve driver performance at the additional integrated circuit.